

# TRANSISTOR ARRAY AND METHOD OF LAYOUT

## ABSTRACT OF THE DISCLOSURE

The present invention discloses a transistor array and a layout method, the array  
5 including a plurality of first LSB transistors arranged along diagonal directions of a  
central portion of a first quadrant of an array including a plurality of rows and a plurality  
of columns; a plurality of first MSB transistors arranged along diagonal directions above  
and below the plurality of first LSB transistors, respectively; a plurality of second LSB  
transistors and a plurality of second MSB transistors arranged on a second quadrant of  
10 the array to be symmetrical in a Y-axis direction to the plurality of first LSB transistors  
and the plurality of first MSB transistors; a plurality of third LSB transistors and a  
plurality of third MSB transistors arranged on a third quadrant of the array to be  
symmetrical in an X-axis direction to the plurality of first LSB transistors and the plurality  
of first MSB transistors; and a plurality of fourth LSB transistors and a plurality of fourth  
15 MSB transistors arranged on a fourth quadrant of the array to be symmetrical in a Y-  
axis direction to the plurality of third LSB transistors and the plurality of third MSB  
transistors, such that the transistor array can minimize the effects of temperature  
distribution and process variation.